Silicon Wafer Processing

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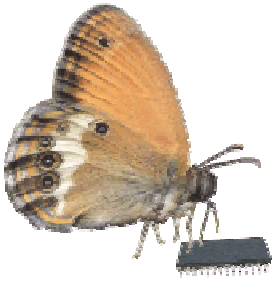

Objective

To provide an overview for manufacturing systems students of the steps and processes required to make integrated circuits from blank silicon wafers.

Goals

The Transfer Plan provides a curriculum covering the process of manufacturing integrated circuits from the silicon wafer blanks, using the equipment manufactured by Applied Materials, Lam Research, and others of its competitors. The curriculum will be modular, with each module covering a process in sequence. This curriculum will be developed for internet access.

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Introduction

The processing of Silicon wafers to produce integrated circuits involves a good deal of chemistry and physics. In order to alter the surface conditions and properties, it is necessary to use both inert and toxic chemicals, specific and unusual conditions, and to manipulate those conditions with both plasma-state elements and with RF (Radio Frequency) energies. Starting with thin, round wafers of silicon crystal, in diameters of 150, 200, and 300mm, the processes described here build up a succession of layers of materials and geometries to produce thousands of electronic devices at tiny sizes, which together function as integrated circuits (ICs). The devices which now occupy the surface of a one-inch square IC would have occupied the better part of a medium-sized room 20 years ago, when all these devices (transistors, resistors, capacitors, and so on) were only available as discreet units.

The conditions under which these processes can work to successfully transform the silicon into ICs require an absolute absence of contaminants. Thus, the process chambers normally operate under vacuum, with elemental, molecular, and other particulate contaminants rigorously controlled. In order to understand these processes, then, we will begin the study of semiconductor processing with an overview of vacuum systems and theory, of gas systems and theory, as applied specifically to these tools, and of clean room processes and procedures

The semiconductor industry reflects and serves an extraordinary revolution in both materials science and in data processing and storage. As recently as 1980, most individuals had no idea that computers would ever impact their personal lives. Today, many families own one or two computers, and use many other computers and dedicated processor systems in their appliances and automobiles. The intrusion of electronics and computer technology into our lives and the devices we use daily is growing at an exponential rate, and Moore's Law still applied in the computer world. This is one of the few markets in which, as time passes, the power and capacity of the products grows steadily, while the cost of that power and capacity drops.

Today, only twenty years later, we are continually pushing the envelope of capabilities of the data processing and storage systems that are now in the mainstream. Ingenuity and creativity, along with great strides in quality control, process control, and worker productivity, are leading daily to new ideas about how to further reduce device size and data density. On the horizon are visions of biochemically-based devices which will be far smaller, work faster, and generate less heat than current devices. It is worth spending some time imagining where this evolving technology will take us, and the society we live in.

Preparation of the Silicon Wafer Media

From: http://www.ade.com/employment/silicon_wafer.html

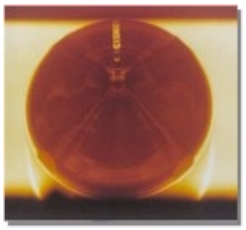
Wafer products are measured at various stages of the process to identify defects inducted by the manufacturing process. This is done to eliminate unsatisfactory wafer materials from the process stream and to sort the wafers into batches of uniform thickness and at a final inspection stage. These wafers will become the basic raw material for new integrated circuits. The following is a summary of the steps in a typical wafer manufacturing process.

Silicon Thermal Properties

Thermal Conductivity (solid) 1.412 W/cm-K
Thermal Conductivity (liquid) 4.3 W/cm-K
Specific Heat 0.70 J/g-K
Thermal Diffusivity .9 cm**2/s
Melting Point 1683 K
Boiling Point 2628 K
Critical Temperature 5159 K
Density (solid) 2.33 g/cm**3
Density (liquid) 2.53 g/cm**3
Vapor pressure
at 1050C 1e-7 Torr
at 1250C 1e-5 Torr
Molar heat capacity 20.00 J/mol-K

Crystal Growth and Wafer Slicing Process

The first step in the wafer manufacturing process is the formation of a large, perfect silicon crystal. The crystal is grown from a 'seed crystal' that is a perfect crystal. The silicon is supplied in granular powder form, then melted in a crucible. The seed is immersed carefully into the crucible of molten silicon, then slowly withdrawn.



Step 1: Obtaining the Sand

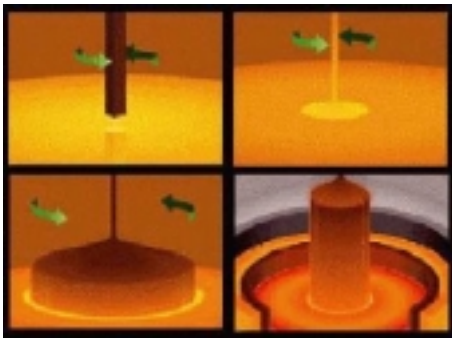
The sand used to grow the wafers has to be a very clean and good form of silicon. For this reason not just any sand scraped off the beach will do. Most of the sand used for these processes is shipped from the beaches of Australia.

Step 2: Preparing the Molten Silicon Bath

The sand (SiO_2)is taken and put into a crucible and is heated to about 1600 degrees C – just above its melting point. The molten sand will become the source of the silicon that will be the wafer.

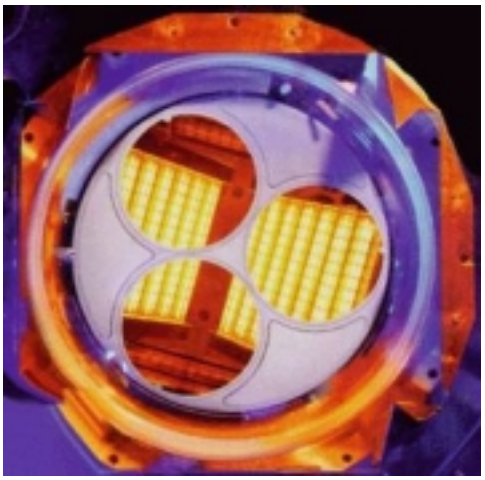
Step 3: Making the Ingot

A pure silicon seed crystal is now placed into the molten sand bath. This crystal will be pulled out slowly as it is rotated. The dominant technique is known as the Czochralski (cz) method. The result is a pure silicon cylinder that is called an ingot. As description or a variant on the Czochralski method is available at http://www.ioi.co.uk/tech/dera/p0526.htm



The Czochralski method

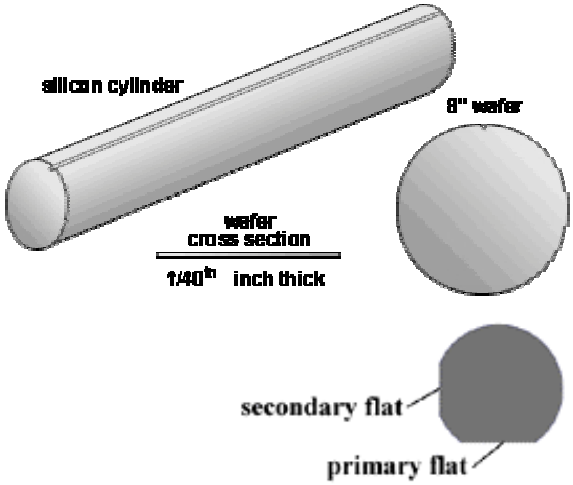
Examples of some completed ingots



An epitaxial reactor.

Growth of Epitaxial Silicon

This step is done to provide a good clean surface for later processing. If a layer of Silicon is grown onto the top of the wafer using chemical methods then that layer is of a much better quality then the slightly damaged or unclean layer of silicon in the wafer. The epitaxial layer is where the actual processing will be done.



The diameter of the silicon ingot is determined by the temperature variables as well as the rate at which the ingot is withdrawn. When the ingot is the correct length, it is removed, then ground to a uniform external surface and diameter.

Each of the wafers is given either a notch or a flat edge that will be used later in orienting the wafer into the exact position for later procedures. In these two figures you can see a notch (above) and flats. Flats in this image are exaggerated for clarity.

Step 4: Preparing the Wafers

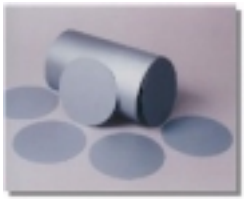
After the ingot is ground into the correct diameter for the wafers, the silicon ingot is sliced into very thin wafers. This is usually done with a diamond saw.

A diamond saw for cutting wafers

Each of these wafers will then go through polishing until they are very smooth and just the right thickness (see Polishing Process, below).

Thickness Sorting

Following slicing, silicon wafers are often sorted on an automated basis into batches of uniform thickness to increase productivity in the next process step, lapping. During thickness sorting, the wafer manufacturer can also identify defect trends resulting from the slicing process.



Lapping & Etching Processes

Lapping removes the surface silicon which has been cracked or otherwise damaged by the slicing process, and assures a flat surface. Wafers are then etched in a chemically active reagent to remove any crystal damage remaining from the previous process step.

Thickness Sorting and Flatness Checking

Following lapping or etching, silicon wafers are measured for flatness to identify and control defect trends resulting from the lapping and etching processes. Wafers are also often sorted on an automated basis according to thickness in order to increase productivity in the next process step, polishing.

Polishing Process

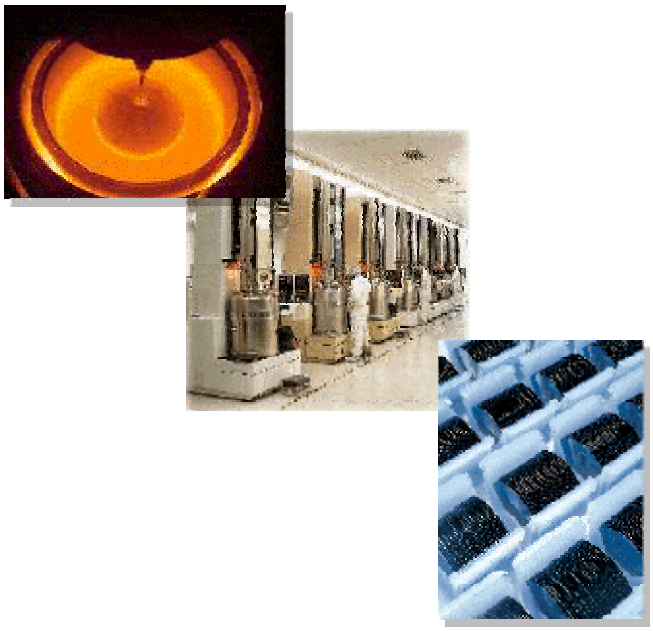
Polishing is a chemical/mechanical process that smoothes the uneven surface left by the lapping and etching processes and makes the wafer flat and smooth enough to support optical photolithography.

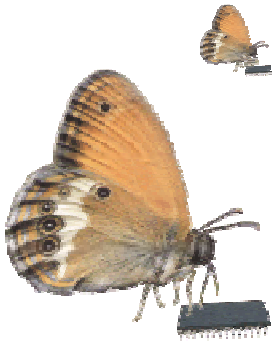
A wafer polishing machine

Wafers in storage trays

Final Dimensional and Electrical Properties Qualification

The wafers undergo a final test, performed in order to demonstrate conformance with customer specification for flatness, thickness, resistivity and type. Process induced defect and defect trend information is used by the wafer manufacturer for yield and process management of the immediately preceding steps. Information regarding surface defects, such as scratches and particles, and defect trend information are used by the wafer manufacturer for yield and process improvement.





Silicon Wafer Processing Steps

Semiconductor manufacturing

from http://www.micron.com/resources/semi_manufacture.htm

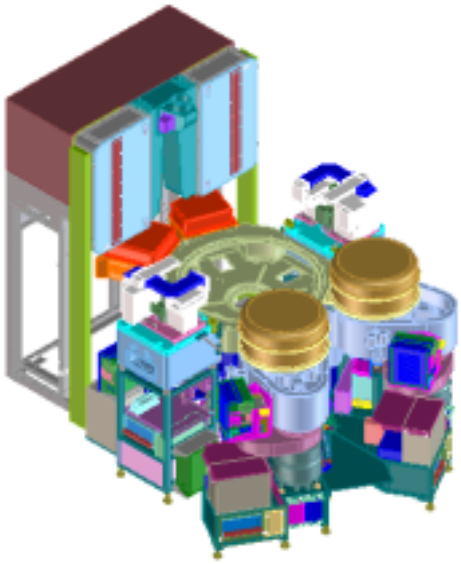
Today, most integrated circuits (ICs) are made of silicon. Turning silicon into memory chips is an exacting, meticulous procedure involving engineers, metallurgists, chemists and physicists. The first step from silicon to circuit is the creation of a pure, single-crystal cylinder or ingot of silicon six to eight inches in diameter. These cylinders are sliced into thin, highly polished wafers less than one-fortieth of an inch thick. Micron uses six- and eight-inch wafers. The circuit elements (transistors, resistors, and capacitors) are built in layers on the silicon wafer. Hundreds of memory chips are etched onto each wafer.

Pure single-crystal cylinders of silicon are sliced into thin, highly polished wafers less than one-fortieth of an inch thick. Hundreds of memory chips are etched onto each wafer, while for processor chips, perhaps only ten to 50 devices will fit on one wafer.

Most chip designs are developed with the help of computer systems or computer-aided design (CAD) systems. Circuits are developed, tested by simulation, and perfected on computer systems before they are actually built. When the design is complete, glass photomasks are made—one mask for each layer of the circuit. These glass photomasks are used in a process called photolithography.

Fabrication

Semiconductor memory chips are manufactured in cleanroom environments because the circuitry is so small even tiny bits of dust can damage it. Class 1 and class 10 cleanrooms are typical. In a class 1 cleanroom, there is no more than 1 particle of dust in a cubic foot of air. In comparison, a clean, modern hospital has about 10,000 dust particles per cubic foot. The air inside a cleanroom is filtered and recirculated continuously, and employees wear special clothing such as dust-free gowns, caps, and masks to help keep the air particle-free.

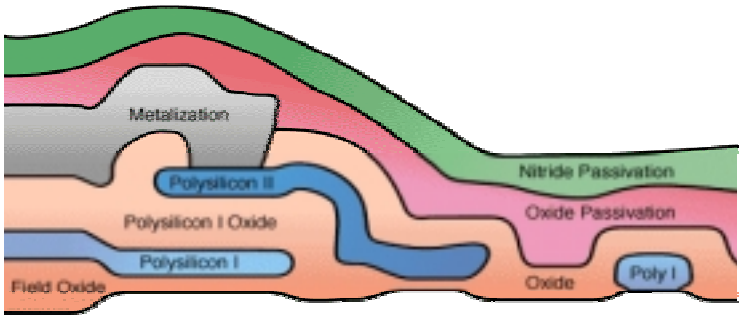


The figure at the right shows a modern semiconductor etch machine. At the top left is the wafer handling system, which accepts wafers from the factory materials handling system, aligns them for processing in the etch machine, and moves them into the main part of the machine. While this system normally operates at atmospheric pressure, it is usually at a

Class 10 clean room level. When wafers move into the process part of the machine, they are contained in a vacuum, with extremely low particle contamination levels (Class 1). Even the smallest particle can ruin an entire wafer, with a large number of integrated circuits affected, and costing hundreds or thousands of dollars.

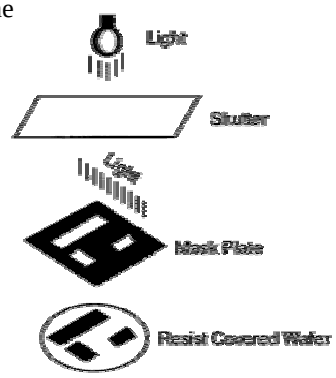
The large circular part in the center of the machine is a transfer area, which moves the wafers between process chambers. The machine shown has four process chamber locations, each one of which can be individually configured depending on the process that is desired.

After processing, the wafers are moved back into the materials handling system and returned to the factory floor. For further processing. A single wafer may have to undergo many succesive process steps to achieve the complex layers of conductor, semiconductor, and insulating material needed to produce the desired circuitry. This process is described below, in outline first, then in more detail.



Layers on a semiconductor device.

Process Steps Outline



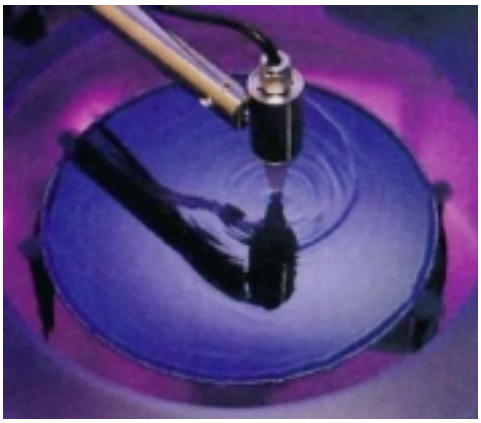
- **Diffusion**. A layer of material such as oxide is grown or deposited onto the wafer.
- **Coat / Bake**. The resist, a light sensitive protective layer, is applied and cured in place.
- **Align**. A reticule is positioned over the wafer. Ultraviolet light shines through the clear portions of the reticule exposing the pattern onto the photosensitive resist.
- **Develop**. The resist is developed and unwanted resist is washed away.
- **Dry Etch**. Dry etch removes oxide not protected by resist.
- **Wet Etch and Clean**. The remaining resist is removed in wet etch to reveal the patterned oxide layer. Then the wafer is cleaned. The process is repeated up to 18 times to create the various layers necessary for each part's circuitry.

Process Steps Details

In this sterile environment, the wafers are exposed to a multiple-step photolithography process that is repeated once for each mask required by the circuit. Each mask defines different parts of a transistor, capacitor, resistor, or connector composing the complete integrated circuit and defines the circuitry pattern for each layer on which the device is fabricated.

At the beginning of the production process, the bare silicon wafer is covered with a thin glass layer followed by a nitride layer. The glass layer is formed by exposing the silicon wafer to oxygen at temperatures of 900 degrees C or higher for an hour or more, depending on how thick a layer is required. Glass (silicon dioxide) is formed in the silicon material by exposing it to oxygen. At high temperatures, this chemical reaction (called oxidation) occurs at a much faster rate.

Photolithography



Next, the wafer is uniformly coated with a thick light-sensitive liquid called photoresist. The coating is applied while the wafer is spinning.

Portions of the wafer are selected for exposure by carefully aligning a mask between an ultraviolet light source and the wafer. In the transparent areas of the mask, light passes through and exposes the photoresist.

Direct Wafer Stepping (DWS)

In this method the mask is quite a bit farther away from the wafer and through a series of optics the image is placed onto the wafer. The main advantage of this method is that the mask can be quite a bit larger then the final pattern and through optical and mechanical manipulations a better resolution can be exposed onto the photoresist. This method is currently the number one method used in industry.

Photoresist hardens and becomes impervious to etchants when exposed to ultraviolet light. This chemical change allows the subsequent developer solution to remove the unexposed photoresist while leaving the hardened, exposed photoresist on the wafer.

Etching the Wafer Surface

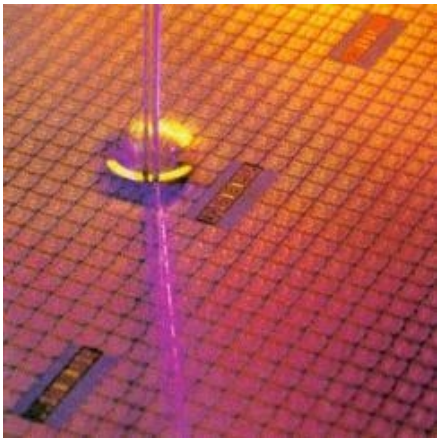
The etching process is used immediately after photolithography to etch the unwanted material from the wafer. This process is not selective and that is why the pattern had to be traced onto the wafer using photoresist. There are two main methods of etching, wet etching and dry etching. This leaves a pattern on the wafer in the exact design of the mask. The hardened photoresist is then removed (cleaned) with another chemical.

Wet Etching

Wet etching is done with the use of chemicals. A batch of wafers is dipped into a higly concentrated pool of acid and the exposed areas of the wafer are etched away. Wet etching is good in that it is fairly cheap and capable of processing many wafers quickly. The disadvantage is that wet etching does not allow the smaller critical geometries that are needed for todays chips.

Acid being poured onto a wafer

A closer look at acid and the wafer.



Dry Etching

Dry etching refers to any of the methods of etching that use gas instead of chemical etchants. Dry etching is capable of producing critical geometries that are very small.

Plasma Etching

Plasma etching uses a gas that is subjected to an intense electric field to generate the plasma state of matter. The electric field is produced with coils that are wrapped around the chamber and exposed to a high level RF source. There are two different versions of this type of etching based on the shape of the chamber used. One consists of a barrel type chamber where the wafers are placed sitting up while the gas is flowed over the wafers and out through an exhaust pipe. The second process uses a parallel plate reactor. There are two plates that are used to give the gas the electric field rather than the coil that is wrapped around the barrel chamber. In plasma form, the gases used are very reactive, providing effective etching of the exposed surface. Plasma etching provides good critical geometry but the wafer can be damaged from the RF radiation.

Reactive Ion Etching

This method works at a lower pressure and uses a combined physical and chemical method to etch the wafer.

Ion Milling

Ion milling uses electric and magnetic fields to cause the plasma ions to form a beam that is used to do the etching. This method is extremely accurate and has the ability to reach very small critical geometries.

Anisotropic Etching vs. Isotropic Etching

Isotropic etching is a problem that results from chemical etching and some forms of dry etching. The result is that the etchant material will etch to the side (laterally) as well as straight down. This can cause some of the material under the patterned resist to be etched away, resulting in undercutting and poor image accuracy. Anisotropic etching occurs in most forms of dry etching. In this process there is no lateral etching so an exact representation of the pattern is etched onto the wafer. Anisotropic etching is more desirable because there can be problems in maintaining the desired electrical characteristics if there is lateral etching as well as vertical etching.

Implant / Masking Steps: Diffusion & Ion Implant

Electrical characteristics of selected areas on the developing integrated circuit are changed by implanting energized ions (dopants) in the form of specific impurities into areas not protected by resist or other layers. The dopants come to rest below the wafer's surface, creating the positive and negative areas on the wafer which encourage or discourage the flow of electrical current throughout the die. These basic steps are repeated for additional layers of polysilicon, glass, and aluminum. Typical dopants include:

- Boron
- Arsenic
- Phosphorous

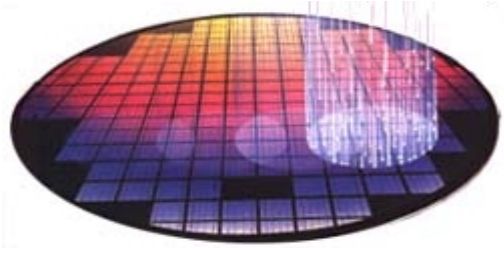
These processes can be damaging to the wafer, so a heating process known as annealing is used to reduce any damage to the wafers.

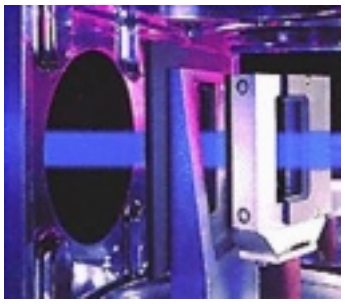
Diffusion

Diffusion is done in a furnace with a flow of gas running over the wafers. This step, like etch, is not selective so the photoresist and patterning need to be done before this step. The best way to understand the processes of this step is to imagine oxidation. Diffusion is very similar to oxidation except using a different gas other than oxygen.

Ion Implantation

Ion implantation is different from diffusion. Diffusion uses the natural state of gas going to where there is no gas, while ion implantation shoots the desired dopant ions into the wafer. Ion implantation has been best equated with firing a machine gun into a wall. In this analogy the wall is the wafer and the bullets are the ions. The main disadvantage of ion implantation is that it can only process a single wafer at a time while a diffusion chamber is capable of handling many wafers.





The magnets used to control the ion beam

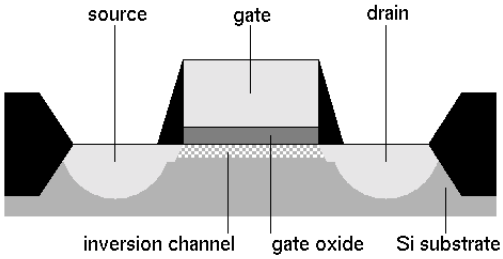
A wafer handling tray in ion implantation

Drive In

This is the next step after the ions have been placed into the wafer. In this step the wafer is heated to make the ions go deeper into the wafer.

Annealing

Due to the incredible damage that these processes (especially ion implantation) can cause to the wafer an additional stage of heating is required. During this final stage the wafer is heated so that the crystal lattice structure of the wafer will repair itself.



The finished wafer is an intricate sandwich of n-type and p-type silicon and insulating layers of glass and silicon nitride.

All of the circuit elements (transistor, resistor, and capacitor) are constructed during the first few mask operations. The next masking steps connect these circuit elements together.

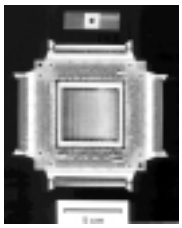
An insulating layer of glass (called BPSG) is deposited and a contact mask is used to define the contact points or windows of each of the circuit elements. After the contact windows are etched, the entire wafer is covered with a thin layer of aluminum in a sputtering chamber. The metal mask is used to define the aluminum layer leaving a fine network of thin metal connections or wires.

The entire wafer is then covered with an insulating layer of glass and silicon nitride to protect it from contamination during assembly. This protective coating is called the passivation layer. The final mask and passivation etch removes the passivation material from the terminals, called bonding pads. The bonding pads are used to electrically connect the die to the metal pins of the plastic or ceramic package.

While still on the wafer, every integrated circuit is tested and functional and nonfunctional chips are identified and mapped into a computer data file. A diamond saw then cuts the wafer into individual chips. Nonfunctional chips are discarded and the rest are sent on to be assembled into plastic packages.

Die Attach / Wire Bond

Before the die are encapsulated, they are mounted on to lead frames, and thin gold wires connect the bonding pads on the chip to the frames to create the electrical path between the die and lead fingers.



Product samples are taken out of the normal product flow for environmental and reliability assurance testing. These quality assurance test push chips to their extreme limits of performance to ensure high-quality, reliable die and to assist engineering with product and process improvements.

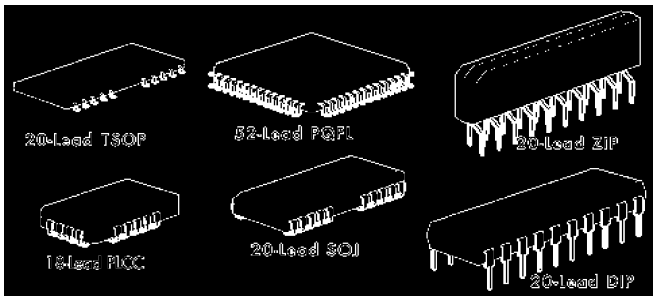
Encapsulation

During Encapsulation, lead frames are placed onto mold plates and heated. Molten plastic material is pressed around each die to form its individual package. The mold is opened, and the lead frames are pressed out and cleaned.

Lead Finish / Trim and Form

Electroplating (illustrated at left) is the next process where the encapsulated lead frames are "charged" while submerged in a tin/lead solution. The tin/lead ions are attracted to the electrically charged leads create a uniform plated deposit which increases the conductivity and provides a clean consistent surface for surface mount applications.

In Trim & Form, lead frames are loaded into trim-and-form machines where the leads are formed step by step until finally the chips are severed from the frames. Individual chips are then put into anti-static tubes for handling and transportation to the test area for final testing.



Various Memory Chip Packaging (the thinnest being the most recent)

The various positions and shapes of the leads and the package size and shape depend on the final application and the customer's packaging requirements.

Final Testing / Shipping

Each memory chip is tested at various stages in the manufacturing process to see how fast it can store or retrieve information, including the high temperature burn-in in Micron's proprietary AMBYX® ovens which test the circuitry of each chip, ensuring the quality and reliability. This monitored burn-in provides feedback throughout the process, allowing identification and correction of manufacturing problems.

The completed packages are inspected, sealed, and marked with a special ink to indicate product type, date, package code, and speed. The finished goods area ships the chips to computer, peripheral, telecommunications, and transportation customers throughout the world.

In the last 30 years semiconductors have become virtually indispensable in many aspects of daily life. Even people who do not own or use a computer are likely to use semiconductor memory in one way or another. Many of the fantastic capabilities of our modern world are possible thanks to the semiconductor memory chip.